PRODUCT RELIABILITY REPORT

Platform: S100E2.0

--100V E-Mode GaN FET

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1. Platform Information

Platform	S100E2.0
BV Rating(V)	100
Process Technology	GaN on Silicon

2. Reliability Tests

Innoscience's E-mode GaN FET was subjected to a variety of reliability tests under the conditions referenced to typical for silicon-based power MOSFET. Spin-off products' device have the same die process and design rules as INN100W032A.

Category	Product Number	Package	BV Rating(V)
Platform	INN100W032A	WLCSP (3.50mm x 2.13mm)	100
Spin-off	INN100FQ016A	FCQFN (4mm x 6mm)	100
Spin-off	INN100FQ025A	FCQFN (3mm x 5mm)	100
Spin-off	INN100W027A	WLCSP (4.45mm x 2.3mm)	100
Spin-off	INN100W070A	WLCSP (2.5mm x 1.5mm)	100

Note: INN100W027A and INN100W070A has same package process and design with INN100W032A；INN100FQ016A and INN100FQ025A as new package type (FCQFN) need to be requalified.

Platform and spin-off product reliability test items and results were shown as below:

Platform Product (INN100W032A)				
Test Items	Test Condition	#Fail	Sample Size (Unit x Lot)	Result
MSL1	T=85°C, RH=85%, 3 x reflow	0 Fail	25 x 3	Pass
HTRB	T=150°C, VD=80V	0 Fail	77 x 3	Pass
HTGB	T=150°C, VG=5.5V	0 Fail	77 x 3	Pass
BLTC	-40 to +125°C, Air	0 Fail	77 x 3	Pass
H^3TRB	T=85°C, RH=85%, VD=80V	0 Fail	77 x 3	Pass
HAST	T=130°C, RH=85%, VD=42V	0 Fail	77 x 3	Pass
HTSL	T=150°C	0 Fail	77 x 3	Pass
HTOL	LLC, Vin=60V, Fsw=1MHz, Tj＞125°C	0 Fail	10 x 3	Pass
HBM	All Pins	0 Fail	3 x 1	Class 1C
CDM	All Pins	0 Fail	3 x 1	Class C3

Spin-off Product-WLCSP				
Test Items	Test Condition	#Fail	Sample Size (Unit x Lot)	Result
MSL1	T=85°C, RH=85%, 3 x reflow	0 Fail	25 x 3	Pass
HTRB	T=150°C, VD=80V	0 Fail	77 x 1	Pass
HTGB	T=150°C, VG=5.5V	0 Fail	77 x 1	Pass
BLTC	-40 to +125°C	0 Fail	77 x 1	Pass
H^3TRB	T=85°C, RH=85%, VD=80V	0 Fail	77 x 1	Pass
HAST	T=130°C, RH=85%, VD=42V	0 Fail	77 x 1	Pass
HTSL	T=150°C	0 Fail	77 x 1	Pass
HTOL	LLC, Vin=60V, Fsw=1MHz, Tj＞125°C	0 Fail	10 x 1	Pass
HBM	All Pins	0 Fail	3 x 1	Class 1C
CDM	All Pins	0 Fail	3 x 1	Class C2a

Spin-off Product-FCQFN				
Test Items	Test Condition	#Fail	Sample Size (Unit x Lot)	Result
MSL3	T=30°C, RH=60%, 3 x reflow	0 Fail	25 x 3	Pass
HTRB	T=150°C, VD=80V	0 Fail	77 x 1	Pass
HTGB	T=150°C, VG=5.5V	0 Fail	77 x 1	Pass
PLTC	-55℃to +150℃	0 Fail	77 x 3	Pass
H^3TRB	T=85°C, RH=85%, VD=80V/120V	0 Fail	77 x 3	Pass
HAST	T=130°C, RH=85%, VD=42V	0 Fail	77 x 3	Pass
HTSL	T=150°C	0 Fail	77 x 3	Pass
Solderability	1.Precondition : 8H 2. Pb-feee,245±5℃,5±0.5S.	0 Fail	10 x 1	Pass
HBM	All Pins	0 Fail	3 x 1	Class 2
CDM	All Pins	0 Fail	3 x 1	Class C3

3. Reliability Tests

Innoscience's E-mode GaN FETs were subjected to a variety of reliability test under the condition referenced to typical for silicon-based power MOSFETs. These test items and results were shown as below:

Moisture Sensitivity Level (MSL)

Parts were baked at 125°C for 24 hours, and then subjected to 85%RH at 85°C for a stress period of 168 hours (or subjected to 30%RH at 60°C for a stress period of 192 hours). The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC standard J-STD-020.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
MSL1	INN100W032A	T=85°C, RH=85%, 3 x reflow	0	25 x 3	168
	INN100W027A	T=85°C, RH=85%, 3 x reflow	0	25 x 3	168
MSL3	INN100FQ016A	T=30°C, RH=60%, 3 x reflow	0	25 x 3	192
	INN100FQ025A	T=30°C, RH=60%, 3 x reflow	0	25 x 3	192

Note: INN100FQ016A Package design & process is same with INN150FQ032A, Package reliability test reference INN150FQ032A.

High Temperature Reverse Bias (HTRB)

Parts were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A108.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTRB	INN100W032A	T=150°C, VD=80V, VG=VS=0V	0	77 x 3	1000
	INN100FQ016A	T=150°C, VD=80V, VG=VS=0V	0	77 x 1	1000
	INN100FQ025A	T=150°C, VD=80V, VG=VS=0V	0	77 x 1	168
	INN100W027A	T=150°C, VD=80V, VG=VS=0V	0	77 x 1	168
	INN100W070A	T=150°C, VD=80V, VG=VS=0V	0	77 x 1	168

High Temperature Gate Bias (HTGB)

Parts were subjected to 5.5V gate-source bias at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A108.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTGB	INN100W032A	T=150°C, VG=5.5V, VD=VS=0V	0	77 x 3	1000
	INN100FQ016A	T=150°C, VG=5.5V, VD=VS=0V	0	77 x 1	1000
	INN100FQ025A	T=150°C, VG=5.5V, VD=VS=0V	0	77 x 1	168
	INN100W027A	T=150°C, VG=5.5V, VD=VS=0V	0	77 x 1	168
	INN100W070A	T=150°C, VG=5.5V, VD=VS=0V	0	77 x 1	168

Temperature Cycling (TC)

Parts were subjected to temperature cycling for a total of 1000 cycles. Heating rate and cooling rate of 15°C/min. Dwell time of 5 minutes were used in accordance with the JEDEC Standard JESD22-A104.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Cycles)
BLTC	INN100W032A	-40 to +125°C, Air	0	77 x 3	1000
	INN100W027A	-40 to +125°C, Air	0	77 x 1	500
PLTC	INN100FQ016A	-55 to +150°C, Air	0	77 x 3	1000
	INN100FQ025A	-55 to +150°C, Air	0	77 x 3	1000

Note: INN100FQ016A Package design & process is same with INN150FQ032A, Package reliability test reference INN150FQ032A.

High Humidity, High Temperature Reverse Bias (H3TRB)

Parts were subjected to 80% of the rated drain-source bias at 85%RH and 85°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A101.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
H^3TRB	INN100W032A	T=85°C, RH=85%, VD=80V, VG=VS=0V	0	77 x 3	1000
	INN100FQ016A	T=85°C, RH=85%, VD=120V, VG=VS=0V	0	77 x 3	1000
	INN100FQ025A	T=85°C, RH=85%, VD=80V, VG=VS=0V	0	77 x 3	1000
	INN100W027A	T=85°C, RH=85%, VD=80V, VG=VS=0V	0	77 x 1	168

Note: INN100FQ016A Package design & process is same with INN150FQ032A, Package reliability test reference INN150FQ032A.

Highly Accelerated Temperature and Humidity Stress Test (HAST)

Parts were subjected to 42V bias at 85%RH and 130°C for a stress period of 96 hours. The testing was done in accordance with the JEDEC Standard JESD22-A110.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HAST	INN100W032A	T=130°C, RH=85%, VD=42V, VG=VS=0V	0	77 x 3	96
	INN100FQ016A	T=130°C, RH=85%, VD=42V, VG=VS=0V	0	77 x 3	96
	INN100FQ025A	T=130°C, RH=85%, VD=42V, VG=VS=0V	0	77 x 3	96
	INN100W027A	T=130°C, RH=85%, VD=42V, VG=VS=0V	0	77 x 1	96

Note: INN100FQ016A Package design & process is same with INN150FQ032A, Package reliability test reference INN150FQ032A.

High Temperature Storage Life (HTSL)

Parts were subjected to 150°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A103.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTSL	INN100W032A	T=150°C	0	77 x 3	1000
	INN100FQ016A	T=150°C	0	77 x 3	1000
	INN100FQ025A	T=150°C	0	77 x 3	1000
	INN100W027A	T=150°C	0	77 x 1	168

Note: INN100FQ016A HTSL test reference INN150FQ032A.

Dynamic High Temperature Operating Life (DHTOL)

Parts were subjected to DC-to-DC system test adapted Full-bridge LLC topology with V_{IN} =60V bias and F_{SW}=1MHz at junction temperature>125°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. Plan.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
DHTOL	INN100W032A	LLC, Vin=60V, Fsw=1MHz, Tj > 125°C	0	10 x 3	1000
	INN100W027A	LLC, Vin=60V, Fsw=1MHz, Tj > 125°C	0	10 x 1	168

Solderability

Parts were subjected to surface mount process then reflow test. The testing was done in accordance with theJ-STD-002.

Pass criteria: Wetting area > 95%.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)
Solderability	INN100FQ025A	1. Precondition: 8H 2. Pb-feee, 245±5°C, 5±0.5S.	0	10 x 1

Electro-Static Discharge (ESD)

Parts were subjected to HBM (ESDA/JEDEC JS-001) and CDM (ESDA/JEDEC JS-002) test to guarantee that the device can with stand electrostatic voltages during handling.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	Passed Voltage	JEDEC Class
HBM	INN100W032A	All Pins	(±) 1500V	Class 1C
CDM	INN100W032A	All Pins	(±) 1000V	Class C3
HBM	INN100W027A	All Pins	(±) 1500V	Class 1C
CDM	INN100W027A	All Pins	(±) 500V	Class C2a
HBM	INN100W070A	All Pins	(±) 1500V	Class 1C
CDM	INN100W070A	All Pins	(±) 500V	Class C2a
HBM	INN100FQ025A	All Pins	(±) 2000V	Class 2
CDM	INN100FQ025A	All Pins	(±) 1000V	Class C3
HBM	INN100FQ016A	All Pins	(±) 2000V	Class 2
CDM	INN100FQ016A	All Pins	(±) 1000V	Class C3

Parts were mounted on to FR4 adaptor cards. Adaptor cards with two copper layers were used. The copper layer thickness was between 1 and 2 oz. SAC305 solder was used to mount the DUTs onto the adaptor cards.

Revision/Updated History

Revision	Reason for Change	Date	Prepared by	Approved by
1.0	Final release	May./17/2022	Mengjin Hu	Blanck, Director
1.1	Add INN100W070A	Feb./7/2023	David Liao/ Huahui Wang	Blanck, Director
1.2	Add INN100W027A	Feb./21/2023	David Liao/ Huahui Wang	Blanck, Director
1.3	Add INN100FQ016A INN100FQ025A	Jul./12/2023	David Liao	Blanck, Director